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10/656,986	09/04/2003	Shin-Rung Lu	67,200-1145	9353

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TUNG & ASSOCIATES  
Suite 120  
838 W. Long Lake Road  
Bloomfield Hills, MI 48302

EXAMINER

DOTY, HEATHER ANNE

ART UNIT PAPER NUMBER

2813

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/656,986

Applicant(s)

LU ET AL.

Examiner

Heather A. Doty

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Aoki et al. (U.S. 5,298,761).

Regarding claim 1, Aoki et al. teaches a method for exposing a blanket photoresist layer comprising providing a substrate having formed thereover a photoresist layer (column 8, lines 40-44; column 16, lines 61-64); and exposing within a single die region within the photoresist layer a minimum of two non-overlapping die sub-patterns while employing a minimum of two masks, each of said masks associated with one of said non-overlapping die sub-patterns (column 8, lines 44-64; Fig. 1a shows the patterns, in a single die area, not overlapping).

Regarding claim 3, Aoki et al. teaches the method of claim 1, and further teaches that the substrate is a ceramic (glass—column 8, lines 40-44) substrate.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Eguchi (U.S. 6,220,714).

Regarding claim 2, Aoki et al. teaches the method of claim 1 (note 35 U.S.C. 102(b) rejection above), but does not teach that the substrate is a semiconductor substrate.

However, Eguchi teaches that liquid crystal devices, such as the one taught by Aoki et al., can be made on glass or silicon substrates (column 16, lines 58-64).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Aoki et al., and also taught by claim 1, and further use a semiconductor substrate, since Eguchi teaches that either glass or silicon is appropriate in such an application.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1).

Regarding claims 4 and 5, Aoki et al. teaches the method of claim 1 (note 35 U.S.C. 102(b) rejection above), but does not specify that the photoresist is either positive or negative photoresist.

Wolf et al. teaches that positive or negative photoresist is appropriate to use in optical lithography (page 408, paragraph 2).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to perform the photolithography methods taught by Aoki et al. and by claim 1, using either positive or negative photoresist, as taught by Wolf et al. The

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motivation for using positive photoresist would be that it has higher resolution capabilities than negative photoresist, as expressly taught by Wolf et al. (page 408, paragraph 2). The motivation for using negative photoresist would be that it is less costly than positive photoresist, as expressly taught by Wolf et al. (page 420, second full paragraph).

Claims 6, 8, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Shibuya et al. (U.S. 5,851,707).

Regarding claims 6, 8 and 13, Aoki et al. teaches a method for exposing a photoresist layer comprising providing a ceramic (glass) substrate—further limited by claim 8—having formed thereover a photoresist layer (column 8, lines 40-44; column 16, lines 61-64); and exposing within a single die region within the photoresist layer a minimum of two non-overlapping die sub-patterns while employing a minimum of two masks, each of said masks associated with one of said non-overlapping die sub-patterns (column 8, lines 44-64; Fig. 1a shows the patterns, in a single die area, not overlapping).

Aoki et al. does not teach employing a minimum of two exposure conditions.

Shibuya et al. teaches using a minimum of two exposure conditions, including illumination (further limited by claim 13; column 1, lines 36-39) to expose different die sub-patterns because some die sub-patterns require finer resolution than others (column 1, lines 24-40).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Aoki et al. and further use a

minimum of two exposure conditions, including illumination, as taught by Shibuya et al., in order to provide different sub-patterns with different levels of resolution, as expressly taught by Shibuya et al.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Shibuya et al. (U.S. 5,851,707) as applied to claim 6 above, and further in view of Eguchi (U.S. 6,220,714).

Regarding claim 7, Aoki et al. and Shibuya et al. together teach the method of claim 6 (note 35 U.S.C. 103(a) rejection above), but do not teach that the substrate is a semiconductor substrate.

However, Eguchi teaches that liquid crystal devices, such as the one taught by Aoki et al., can be made on glass or silicon substrates (column 16, lines 58-64).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Aoki et al. and Shibuya et al. together, and also taught by claim 6, and further use a semiconductor substrate, since Eguchi teaches that either glass or silicon is appropriate in such an application.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Shibuya et al. (U.S. 5,851,707) as applied to claim 6 above, and further in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1).

Regarding claims 9 and 10, Aoki et al. and Shibuya et al. together teach the method of claim 6 (note 35 U.S.C. 103(a) rejection above), but do not specify that the photoresist is either positive or negative photoresist.

Wolf et al. teaches that positive or negative photoresist is appropriate to use in optical lithography (page 408, paragraph 2).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to perform the photolithography methods taught by Aiko et al. and Shibuya et al. together, and by claim 6, using either positive or negative photoresist, as taught by Wolf et al. The motivation for using positive photoresist would be that it has higher resolution capabilities than negative photoresist, as expressly taught by Wolf et al. (page 408, paragraph 2). The motivation for using negative photoresist would be that it is less costly than positive photoresist, as expressly taught by Wolf et al. (page 420, second full paragraph).

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Shibuya et al. (U.S. 5,851,707) as applied to claim 6 above, and further in view of Lai et al. (U.S. 6,187,486).

Regarding claims 11 and 12, Aoki et al. and Shibuya et al. together teach the method of claim 6 (note 35 U.S.C. 103(a) rejection above). They do not teach that the exposure conditions include exposure energy or depth of focus.

Lai et al. teaches that exposure energy and depth of focus are exposure conditions that affect the linewidth of the exposed photoresist (column 1, lines 48-67).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Aoki et al. and Shibuya et al. together, and further use a minimum of two exposure conditions including exposure

energy and depth of focus, in order to modify the linewidth of the photoresist patterns, as taught by Lai et al., for the various sub-pattern exposures.

Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Lee et al. (U.S. 2004/0197964).

Regarding claims 14 and 16, Aoki et al. teaches a method for forming a patterned layer comprising providing a ceramic (glass) substrate—further limited by claim 16—having formed thereover a photoresist layer (column 8, lines 40-44; column 16, lines 61-64); and exposing within a single die region within the photoresist layer a minimum of two non-overlapping die sub-patterns while employing a minimum of two masks, each of said masks associated with one of said non-overlapping die sub-patterns (column 8, lines 44-64; Fig. 1a shows the patterns, in a single die area, not overlapping); and developing the exposed photoresist layer to form a patterned photoresist layer (column 19, lines 32-38).

Aoki et al. further teaches that this method can be used to form a liquid crystal device, but does not expressly teach forming a target layer over the substrate or processing the target layer to form a processed target layer while employing the patterned photoresist layer as a mask layer.

Lee et al. teaches a method of forming a liquid crystal device comprising forming a target layer (transparent conductor, **22** in Fig. 5); and processing the target layer to form a processed target layer while employing a photoresist layer as a mask (paragraph 0033; Fig. 5).



Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Aoki et al. and Lee et al. by first forming a target layer over the substrate, as taught by Lee et al., then performing the method taught by Aoki et al., and then processing the target layer to form a processed target layer while employing the patterned photoresist as a mask layer, as taught by Lee et al., since this step is known in the art of liquid crystal device processing, and photoresist is well known as an effective etch mask.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Lee et al. (U.S. 2004/0197964) as applied to claim 14 above, and further in view of Eguchi (U.S. 6,220,714).

Regarding claim 15, Aoki et al. and Lee et al. together teach the method of claim 15 (note 35 U.S.C. 103(a) rejection above), but do not teach that the substrate is a semiconductor substrate.

However, Eguchi teaches that liquid crystal devices, such as the one taught by Aoki et al., can be made on glass or silicon substrates (column 16, lines 58-64).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Aoki et al. and Lee et al. together, and also taught by claim 14, and further use a semiconductor substrate, since Eguchi teaches that either glass or silicon is appropriate in such an application.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Lee et al. (U.S. 2004/0197964) as applied to

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claim 14 above, and further in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1).

Regarding claims 17 and 18, Aoki et al. and Shibuya et al. together teach the method of claim 14 (note 35 U.S.C. 103(a) rejection above), but do not specify that the photoresist is either positive or negative photoresist.

Wolf et al. teaches that positive or negative photoresist is appropriate to use in optical lithography (page 408, paragraph 2).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to perform the photolithography methods taught by Aiko et al. and Lee et al. together, and by claim 14, using either positive or negative photoresist, as taught by Wolf et al. The motivation for using positive photoresist would be that it has higher resolution capabilities than negative photoresist, as expressly taught by Wolf et al. (page 408, paragraph 2). The motivation for using negative photoresist would be that it is less costly than positive photoresist, as expressly taught by Wolf et al. (page 420, second full paragraph).

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. 5,298,761) in view of Lee et al. (U.S. 2004/0197964) as applied to claim 14 above, and further in view of Shibuya et al. (U.S. 5,851,707).

Regarding claims 19 and 20, Aoki et al. and Lee et al. together teach the method of claim 14 (note 35 U.S.C. 103(a) rejection above), but do not teach employing at least two separate exposure conditions.

Shibuya et al. teaches using a minimum of two exposure conditions, including illumination (further limited by claim 20; column 1, lines 36-39) to expose different die sub-patterns because some die sub-patterns require finer resolution than others (column 1, lines 24-40).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Aoki et al. and Lee et al. and further use a minimum of two exposure conditions, including illumination, as taught by Shibuya et al., in order to provide different sub-patterns with different levels of resolution, as expressly taught by Shibuya et al.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

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published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800